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EXAMINER
MAI, TAN V

ART UNIT	PAPER NUMBER
2124	7

DATE MAILED: 08/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/703,140	Applicant(s) HOYLE, DAVID	
	Examiner Tan V Mai	Art Unit 2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *14 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. Applicant's election of Group I, Claims 1-7 and 9-11, in Paper No. 6 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. The disclosure is objected to because of the following informalities:

In the specification, pages 19 and 28; the status of Co-pending Applications is required to be kept current.

Appropriate correction is required.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Purcell '070 in view of either Balkanski et al or Saishi et al.

As per independent claim 1, Purcell discloses, e.g., see Figs. 1 and 2, the invention substantially as claimed, including: either multipliers (120, 121) & concatenation port (124) of Fig. 1 or multipliers (232, 231) & concatenation port (244) of Fig. 2 which are capable of performing the claimed "forming" and "combining" steps, respectively. It is noted that Purcell does NOT specifically disclose: (1) "fetching", (2)

"rounding" and (3) "shifting" steps. Firstly, the input words A and B [of Purcell] should be stored in memory means. Secondly, the "rounding" and "shifting" steps are old and well known in the art to round and truncate a "result" to a desired length. For example, (1) Balkanski et al (e.g., see Fig.1 element 18; col. 9, lines 11-27) and (2) Saishi et al (e.g., see Figs. 1-2 & 8-9, and col. 2, lines 5-41: col. 5, line 51 to col. 6, line 53; col. 8, line 12 to col. 9, line 60) discloses multiplication devices having "rounding" feature (i.e., add a rounding value) and "shifting" feature (i.e., shift or discard a number of bit(s)). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine either Balkanski et al or Saishi et al's "rounding" and "shifting" features in Purcell, thereby making the claimed invention, because the proposed device is a multiplication device having a dual path for most significant product & least significant product and "rounding" & "shifting" features as claimed.

As per claims 2-3, Balkanski et al (e.g., see col. 9, lines 25-26) and Saishi et al (e.g., see col. 2, lines 5-24) do show the claimed feature.

As per claim 4, Balkanski et al (e.g., see col. 9, lines 23-27, "a **1** is added at position **bit 14** in order to round up the number represented by bits 31 through 15. The six most significant bits and the **fifteen least significant bits** of this 32-bit multiplication result are then discarded". It implies "rounding value" 2**14 and shift amount of 15) and Saishi et al (e.g., see Figs. 8 & 9 and col. 2, lines 5-24) do show the claimed feature.

As per claim 5, Balkanski et al do show the claimed feature "fix value of fourteen". Saishi et al (e.g., see col. 2, lines 5-24) do show shifting a number of bits.

As per claim 6, Purcell does show the claimed feature.

Due to the similarity of apparatus claim 9 to method claim 1, it is rejected under a similar rationale.

As per claim 10, Balkanski et al (e.g., see col. 9, lines 23-25, "a **1** is added at position **bit 14** in order to round up the number represented by bits 31 through 15". It implies "rounding value" 2**14) and Saishi et al (e.g., see Figs. 8 & 9 and col. 2, lines 5-24) do show the claimed feature.

As per claim 11, the claim adds "cellular telephone" feature. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine either Balkanski et al or Saishi et al's "rounding" and "shifting" features in Purcell and use in "cellular telephone" as claimed because the proposed device can be implemented in IC and use in "cellular telephone".

5. Claims 1-6 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Purcell '622 in view of either Balkanski et al or Saishi et al.

As per independent claim 1, Purcell discloses, e.g., see Figs. 2, 7 & 9; abstract, last four lines, the invention substantially as claimed, including: either multipliers (232, 231) & concatenation port (244) of Fig. 2 or multipliers (518, 520) & an adder (532) of Fig. 7 which are capable of performing the claimed "forming" and "combining" steps, respectively. It is noted that Purcell does NOT specifically disclose: (1) "fetching", (2) "rounding" and (3) "shifting" steps. Firstly, the input words A and B [of Purcell] should be stored in memory means. Secondly, the "rounding" and "shifting" steps are old and well known in the art to round and truncate a "result" to a desired length. For example, (1) Balkanski et al (e.g., see Fig.1 element 18; col. 9, lines 11-27) and (2) Saishi et al (e.g., see Figs. 1-2 & 8-9, and col. 2, lines 5-41: col. 5, line 51 to col. 6, line 53; col. 8, line 12 to col. 9, line 60) discloses multiplication devices having "rounding" feature (i.e., add a rounding value) and "shifting" feature (i.e., shift or discard a number of bit(s)). It

would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine either Balkanski et al or Saishi et al's "rounding" and "shifting" features in Purcell, thereby making the claimed invention, because the proposed device is a multiplication device having a dual path for most significant product & least significant product and "rounding" & "shifting" features as claimed.

As per claims 2-3, Balkanski et al (e.g., see col. 9, lines 25-26) and Saishi et al (e.g., see col. 2, lines 5-24) do show the claimed feature.

As per claim 4, Balkanski et al (e.g., see col. 9, lines 23-27, "a **1** is added at position **bit 14** in order to round up the number represented by bits 31 through 15. The six most significant bits and the **fifteen least significant bits** of this 32-bit multiplication result are then discarded". It implies "rounding value" 2**14 and shift amount of 15) and Saishi et al (e.g., see Figs. 8 & 9 and col. 2, lines 5-24) do show the claimed feature.

As per claim 5, Balkanski et al do show the claimed feature "fix value of fourteen". Saishi et al (e.g., see col. 2, lines 5-24) do show shifting a number of bits.

As per claim 6, Purcell does show the claimed feature.

Due to the similarity of apparatus claim 9 to method claim 1, it is rejected under a similar rationale.

As per claim 10, Balkanski et al (e.g., see col. 9, lines 23-25, "a **1** is added at position **bit 14** in order to round up the number represented by bits 31 through 15". It implies "rounding value" 2**14) and Saishi et al (e.g., see Figs. 8 & 9 and col. 2, lines 5-24) do show the claimed feature.

As per claim 11, the claim adds "cellular telephone" feature. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine either Balkanski et al or Saishi et al's "rounding" and "shifting" features in

Purcell and use in "cellular telephone" as claimed because the proposed device can be implemented in IC and use in "cellular telephone".

6. Claims 1-6 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al in view of either Balkanski et al or Saishi et al.

As per independent claim 1, Murakami et al disclose, e.g., see Figs. 28 & 29b, the invention substantially as claimed, including: registers (A, B), multipliers and adders of Fig. 28 which are capable of performing the claimed "fetching", "forming" and "combining" steps, respectively. It is noted that Murakami et al do NOT specifically disclose: (1) "rounding" and (2) "shifting" steps; however, the "rounding" and "shifting" steps are old and well known in the art to round and truncate a "result" to a desired length. For example, (1) Balkanski et al (e.g., see Fig.1 element 18; col. 9, lines 11-27) and (2) Saishi et al (e.g., see Figs. 1-2 & 8-9, and col. 2, lines 5-41: col. 5, line 51 to col. 6, line 53; col. 8, line 12 to col. 9, line 60) discloses multiplication devices having "rounding feature (i.e., add a rounding value) and "shifting" feature (i.e., shift or discard a number of bit(s)). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine either Balkanski et al or Saishi et al's "rounding" and "shifting" features in Murakami et al, thereby making the claimed invention, because the proposed device is a multiplication device having a dual path for most significant product & least significant product and "rounding" & "shifting" features as claimed.

As per claims 2-3, Balkanski et al (e.g., see col. 9, lines 25-26) and Saishi et al (e.g., see col. 2, lines 5-24) do show the claimed feature.

As per claim 4, Balkanski et al (e.g., see col. 9, lines 23-27, "a **1** is added at position **bit 14** in order to round up the number represented by bits 31 through 15. The six most significant bits and the **fifteen least significant bits** of this 32-bit multiplication result are then discarded". It implies "rounding value" 2**14 and shift amount of 15) and Saishi et al (e.g., see Figs. 8 & 9 and col. 2, lines 5-24) do show the claimed feature.

As per claim 5, Balkanski et al do show the claimed feature "fix value of fourteen". Saishi et al (e.g., see col. 2, lines 5-24) do show shifting a number of bits.

As per claim 6, Murakami et al do show the claimed feature.

Due to the similarity of apparatus claim 9 to method claim 1, it is rejected under a similar rationale.

As per claim 10, Balkanski et al (e.g., see col. 9, lines 23-25, "a **1** is added at position **bit 14** in order to round up the number represented by bits 31 through 15". It implies "rounding value" 2**14) and Saishi et al (e.g., see Figs. 8 & 9 and col. 2, lines 5-24) do show the claimed feature.

As per claim 11, the claim adds "cellular telephone" feature. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine either Balkanski et al or Saishi et al's "rounding" and "shifting" features in Murakami et al and use in "cellular telephone" as claimed because the proposed device can be implemented in IC and use in "cellular telephone".

7. Claims 1-7 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al in view of either Balkanski et al or Saishi et al.

As per independent claim 1, Yu et al disclose, e.g., see Figs. 1C, 2B & 5, the invention substantially as claimed, including: registers (A-B, C-D), multipliers and

adders of Figurires which are capable of performing the claimed "fetching", "forming" and "combining" steps, respectively. It is noted that Yu et al do NOT specifically disclose: (1) "rounding" and (2) "shifting" steps; however, the "rounding" and "shifting" steps are old and well known in the art to round and truncate a "result" to a desired length. For example, (1) Balkanski et al (e.g., see Fig.1 element 18; col. 9, lines 11-27) and (2) Saishi et al (e.g., see Figs. 1-2 & 8-9, and col. 2, lines 5-41; col. 5, line 51 to col. 6, line 53; col. 8, line 12 to col. 9, line 60) discloses multiplication devices having "rounding" feature (i.e., add a rounding value) and "shifting" feature (i.e., shift or discard a number of bit(s)). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine either Balkanski et al or Saishi et al's "rounding" and "shifting" features in Yu et al, thereby making the claimed invention, because the proposed device is a multiplication device having a dual path for most significant product & least significant product and "rounding" & "shifting" features as claimed.

As per claims 2-3, Balkanski et al (e.g., see col. 9, lines 25-26) and Saishi et al (e.g., see col. 2, lines 5-24) do show the claimed feature.

As per claim 4, Balkanski et al (e.g., see col. 9, lines 23-27, "a **1** is added at position **bit 14** in order to round up the number represented by bits 31 through 15. The six most significant bits and the **fifteen least significant bits** of this 32-bit multiplication result are then discarded". It implies "rounding value" 2**14 and shift amount of 15) and Saishi et al (e.g., see Figs. 8 & 9 and col. 2, lines 5-24) do show the claimed feature.

As per claim 5, Balkanski et al do show the claimed feature "fix value of fourteen". Saishi et al (e.g., see col. 2, lines 5-24) do show shifting a number of bits.

As per claim 6, Yu et al do show the claimed feature.

As per claim 7, Yu et al do show the claimed feature, e.g., see col. 6, line 62 to col. 7, line 7.

Due to the similarity of apparatus claim 9 to method claim 1, it is rejected under a similar rationale.

As per claim 10, Balkanski et al (e.g., see col. 9, lines 23-25, "a **1** is added at position **bit 14** in order to round up the number represented by bits 31 through 15". It implies "rounding value" 2**14) and Saishi et al (e.g., see Figs. 8 & 9 and col. 2, lines 5-24) do show the claimed feature.

As per claim 11, the claim adds "cellular telephone" feature. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine either Balkanski et al or Saishi et al's "rounding" and "shifting" features in Yu et al and use in "cellular telephone" as claimed because the proposed device can be implemented in IC and use in "cellular telephone".

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cited references are art of interest.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan V. Mai whose telephone number is (703) 305-9761. The examiner can normally be reached on Tue-Fri from 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki, can be reached on (703) 305-9662. The fax phone numbers for the organization where this application or proceeding is assigned are:

After-final (703) 746-7238

Official (703) 746-7239

Non-Official/Draft (703) 746-7240.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

TAN V. MAI
PRIMARY EXAMINER